Performance of Ku-Band On-Chip Matched Si Monolithic Amplifiers Using 0.18-μm-Gatelength MOSFETs

Hitoshi Yano, Yasushi Nakahara, Tomohisa Hirayama, Noriaki Matsuno, Yasuyuki Suzuki, and Akio Furukawa

***Abstract*—We demonstrated Ku-band (12–20 GHz) Si MOSFET monolithic amplifiers with on-chip matching networks. In these amplifiers, we used 3-μm-thick Al–metal transmission lines on 8-μm-thick polyimide–SiON–SiO_2 isolation layers for the matching networks. The amplifier showed a gain of 6–10 dB and a noise figure (NF) of 3.5–4 dB up to about 20 GHz, the highest gain and lowest NF yet reported for MOSFET amplifiers at this frequency. We also clarified the lossy on-chip inductor effect on the gain and noise performance of the amplifiers.**

***Index Terms*—Amplifier, CMOS LSI, dielectric quasi-TEM mode, Ku-band, MMIC, on-chip matching, Si MOSFET.**

I. Introduction

SUB-QUARTER-MICROMETER-GATELENGTH Si MOSFETs developed for digital large-scale integrated circuits (LSIs) offer high performance characteristics, such as a high cutoff frequency (f_T) and a maximum oscillation frequency ($f_{\max}$) of over 40 GHz [1]. They also offer a 2.4-Gb/s transmission rate as optical receiver integrated circuits (ICs) [2]. These MOSFETs now have potential for use in RF applications, such as amplifiers that operate in the microwave frequency range.

To apply such Si MOSFETs in gigahertz RF monolithic microwave integrated circuits (MMICs), optimum matching networks are necessary to overcome the limit of the gain–bandwidth (GB) product of the amplifier [3]. Unfortunately, networks on low-resistivity Si substrates have been reported to be lossy [4]. Thus, GaAs-based MMICs on semiinsulating highly resistive substrates have generally been developed instead [7].

However, Si MOSFETs RF ICs are still attractive both because they cost less than GaAs ICs, due to the more mature digital IC process, and also because they can be merged with Si–MOSFET baseband circuits. Several approaches have been taken to avoid the loss due to substrate conductivity: e.g., using a high-resistivity Si substrate [5], a silicon-on-insulator (SOI) substrate [6], coplanar inductors [4], and three-dimensional (3-D) masterslice MMIC technology [3].

We applied inductors on thick polyimide–SiN–SiO_2 isolation layers for on-chip matched Si MOSFET amplifiers and obtained good-performance MMICs in the 4-, 6-, and 12–20-GHz regions [8], [9]. In this paper, we describe how high-performance Si–MOSFET monolithic amplifiers can be achieved, even with matching networks on a low-resistivity lossy Si substrate.

First, we describe the fabrication process for the thick polyimide–SiON–SiO_2 layers on which the matching networks are constructed. We also examine the performance of a sub-quarter-micrometer-gatelength Si MOSFET, its noise parameters, and its small-signal equivalent circuit.

Second, we discuss the transmission-line properties on a lossy Si substrate. We demonstrate that the parameters of equivalent circuits for the transmission lines can be calculated from the usual microstrip-line model with a small modification. We also show that the equivalent circuits can predict the noise properties of the transmission lines.

Third, we demonstrate single-gate MOSFET and cascode-connected MOSFET amplifiers with on-chip matching networks for the Ku-band (10–20 GHz) and compare the measured performance of these amplifiers to results from a simulation based on the transmission-line and MOSFET models.

II. Fabrication Process

The resistivity of the 640-μm-thick Si substrate used for our IC was about 5 $\Omega \cdot$ cm, which is typical for CMOS LSI devices. A standard CMOS LSI fabrication process was used up to the formation of second-level interconnections. At that point, a 1-μm-thick SiON layer was deposited, and then a 4.6-μm-thick polyimide layer, as is generally used for IC passivation, was formed by spin coating. Next, Ti–TiN–Al–TiN layers were deposited by sputtering; the total thickness of the four layers was 3 μm, which was four times the thickness of the second-level metal layer. Third-level interconnections were then formed by dry etching.

III. Device Performance

We developed Ku-band amplifiers by applying 0.18-μm-gatelength nMOSFETs fabricated by a conventional CMOS LSI process. The gate oxide thickness was 3.7 nm. The transconductance was 450 mS/mm.

The gate metal was $CoSi_2$, with a sheet resistance of 9 $\Omega/\square$. Although this is lower than that for gates made of WSi and poly-Si, it was still too high because the cross-sectional area of the gate was not as large as that of the T-shaped gate in a GaAs microwave FET. Therefore, we reduced the gate resistance by

Manuscript received October 17, 2000.

H. Yano, T. Hirayama, N. Matsuno, Y. Suzuki, and A. Furukawa are with the Photonic and Wireless Devices Research Laboratories, System Devices and Fundamental Research, NEC Corporation, Ibaraki 305-8501, Japan (e-mail: h-yano@cq.jp.nec.com).

Y. Nakahara is with ULSI Device Development, NEC Electron Devices, NEC Corporation, Kanagawa 229-1198, Japan.

Publisher Item Identifier S 0018-9480(01)03990-4.

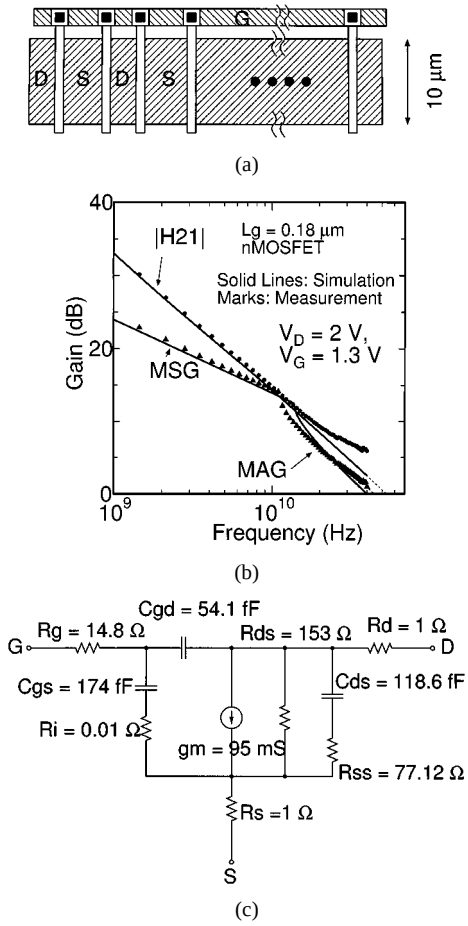


Fig. 1. (a) Typical MOSFET layout. (b) Current gain $|\mathrm{H21}|$, MSG, and MAG plotted versus frequency for an nMOSFET. The gatelength, gate finger length, and total gatewidth of the MOSFET are 0.18, 10, and 200 μm, respectively. Marks represent the measured data, and the solid lines show the simulation data for the equivalent circuit shown in (c) with input/output probe-pad parasitic capacitances. (c) MOSFET equivalent circuit and fitted circuit parameters.

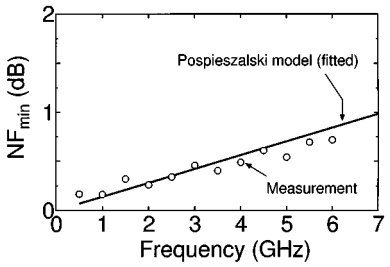


Fig. 2. Measured and fitted $\mathrm{NF_{min}}$ for an nMOSFET with a 200-μm total gatewidth.

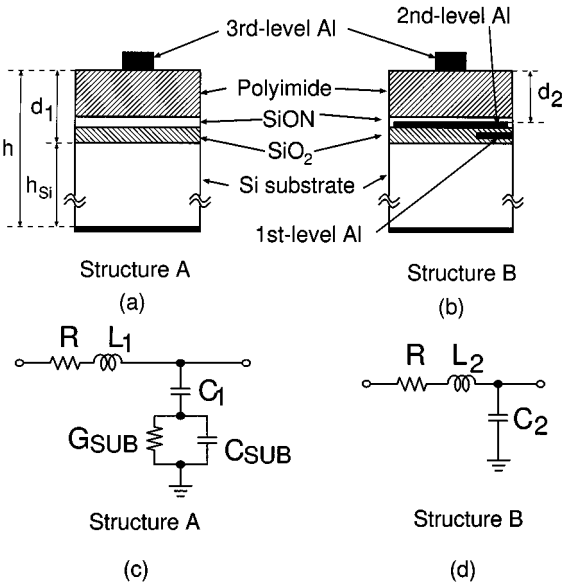


Fig. 3. Cross-sectional view of the transmission lines. The SiO_2 layer was 2.4-μm thick. (a) Structure A. (b) Structure B. (c) Equivalent circuit per unit length for structure A. (d) Equivalent circuit per unit length for structure B.

using a gate electrode consisting of 20 10-μm-long fingers [see Fig. 1(a)].

Fig. 1(b) shows the measured gain-frequency characteristics of an nMOSFET with a 200-μm total gatewidth: f_T determined by extrapolating line $|\mathrm{H21}|$ is 50 GHz, and $f_{\max}$ (where the maximum available gain (MAG) became 0 dB) is 45 GHz. Fig. 1(c) shows an equivalent circuit for the MOSFET and the extracted parameters. The simulated characteristics in Fig. 1(b) were calculated based on the equivalent circuit, including the probe-pad parasitic capacitances. The equivalent gate resistance is 14.8 Ω, which is higher than that of conventional GaAs devices, thus, the transition from maximum stable gain (MSG) to MAG occurred at about 10 GHz. Thus, to apply the MOSFET for amplifier operation in a frequency range above 10 GHz, the series resistance of the input matching networks must be lowered to less than 14.8 Ω to avoid decreasing the MAG of amplifiers with matching networks.

The minimum noise figure ($\mathrm{NF_{min}}$) for the MOSFET was obtained using an on-wafer noise parameter measurement system. The measured $\mathrm{NF_{min}}$ data up to 6 GHz are shown in Fig. 2. The $\mathrm{NF_{min}}$ was well below 1 dB even at 6 GHz. Since the thick isolation layer reduced the capacitive coupling of the Si substrate thermal noise through the probe pad of the MOSFET [8], the measured $\mathrm{NF_{min}}$ very closely represents the intrinsic noise characteristics of the MOSFET.

The $\mathrm{NF_{min}}$ data were fitted to the Pospieszalski model [10], which is well suited for FETs (MESFET, high electron-mobility transistor (HEMT), MOSFET) [11], and we included the parasitics, such as the gate resistance, shown in the equivalent circuit of Fig. 1(c). The extracted gate and drain equivalent noise temperatures T_g and T_d of the Pospieszalski model were 300 and 2800 K, respectively. The solid line in Fig. 2 is the fitted result. The noise parameters extrapolated up to the Ku-band were used to verify our Ku-band amplifier design.

IV. Transmission-Line Properties

The third-level metal layer was used to provide the transmission lines for the matching networks because of its low sheet resistance. We applied two types of cross-sectional structures [see Fig. 3(a) and (b)] in the matching networks. The ground plane for structure A was the bottom of the Si substrate and the ground plane for structure B was the second-level Al layer.

A. Small-Signal Equivalent-Circuit Modeling

When the cross-sectional dimensions of transmission lines are much smaller than the signal wavelength, a quasi-static anal-

ysis can be used to obtain a simple description of the line properties. This makes it easy to obtain an equivalent circuit per unit length, as shown in Fig. 3(d) for structure B, by assuming a quasi-TEM (TEM) field in the cross-sectional area. This quasi-static approach has also been successfully applied for a cross-sectional structure that includes a low-resistivity Si substrate [12]; we thus obtained the equivalent circuit per unit length shown in Fig. 3(c) for structure A. $G_{\rm SUB}$ and $C_{\rm SUB}$ represent the conductance and capacitance, respectively, of the Si substrate.

The equivalent-circuit parameters can be expressed using approximate formulas [14], [15], [17]. We applied these formulas for the Si microstrip lines as follows.

- No skin effect on the transmission lines was assumed, thus, the resistance R was independent of frequency.
- The inductance L_1 was calculated assuming that the ground plane was the bottom of the Si substrate.
- The insulator capacitance C_1 was calculated [16] as

$$C_1 = \varepsilon_1\varepsilon_0\left(W - \frac{\frac{t_{\rm Al}}{2}}{d_1} + \frac{2\pi}{\ln\left(1+\frac{2d_1}{t_{\rm Al}}\left(1+\sqrt{1+\frac{t_{\rm Al}}{d_1}}\right)\right)}\right) \quad (1)$$

  where ε_1 is the relative dielectric constant, ε_0 is the permittivity in a vacuum, and d_1 is the thickness of the insulator. In this formula, the fringing capacitance of the transmission lines is represented by a circular cylinder with diameter $t_{\rm Al}$.
- Since $d_1 \ll h_{\rm Si}$, we calculated the Si substrate capacitance $C_{\rm SUB}$ assuming the transmission line was on top of the Si substrate.
- The substrate conductance $G_{\rm SUB}$ was calculated from $C_{\rm SUB}$ as follows:

$$G_{\rm SUB} = \frac{C_{\rm SUB}}{\varepsilon_{\rm Si}\varepsilon_0\rho_{\rm Si}} \quad (2)$$

  where $\rho_{\rm Si}$ is the resistivity of the Si substrate.
- The capacitance C_2 of structure B was calculated by the same method as C_1. The inductance L_2 was calculated from C_2.

The s-parameters were measured for 1-mm-long transmission lines with different widths for structures A and B. We calculated R, L_1, and L_2 directly from the measured s-parameters at a low frequency, and the other parameters C_1, $C_{\rm SUB}$, $G_{\rm SUB}$, and C_2 were fitted using an MDS HP high-frequency circuit simulator. We also calculated the electrical parameters using the parameters listed in Table I.

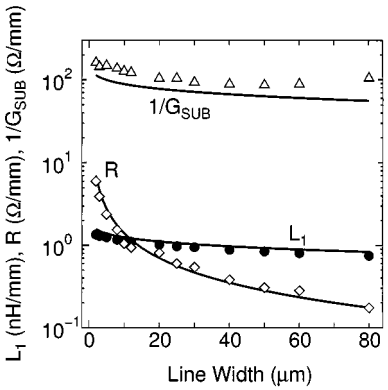
These simple approximations predicted the Si transmission equivalent-circuit parameters fairly well (Figs. 4 and 5). The Si transmission-line models can be easily implemented and used for IC design with the MDS HP circuit simulator.

The transmission-line inductances L_1 and L_2 were quite different between structures A and B. The inductance of structure A was 2.5–9.4 times higher than that of structure B because the Si substrate was a poor magnetic conductor [12].

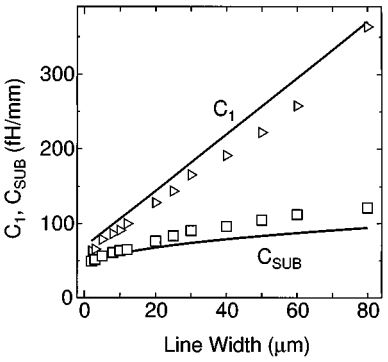
Smith charts for 1-mm-long transmission-line open stubs and shorted stubs are shown in Fig. 6 for structures A and B.

TABLE I
PARAMETERS USED FOR CALCULATION

ρ_{Al}	4.2×10^{-6}	Ωcm
t_{Al}	3	μm
ε_1	3.6	
d_1	8	μm
ε_{Si}	11.9	
h_{Si}	640	μm
ρ_{Si}	5	Ωcm
ε_2	3.4	
d_2	5.6	μm



(a)



(b)

Fig. 4. Calculated and extracted equivalent-circuit parameters for the structure A transmission lines. The solid lines show the calculated parameters, and the marks show the parameters extracted from the measured s-parameters. (a) L_1, R, and $G_{\rm SUB}$. (b) C_1 and $C_{\rm SUB}$.

In the upper part of the Smith chart, the structure A reflection coefficient of the shorted stub, which represents the inductor characteristics, extended farther out than the structure B reflection coefficient. The structure A shorted stub seems not to have been degraded at high frequencies compared to the structure B shorted stub. Our MOSFETs operate in the MAG region in a frequency range above 10 GHz, so the series resistance of the matching network significantly influences an amplifier's gain. Since shorter line with structure A can have the same inductance as a longer lines with structure B (thus resulting in a lower total series resistance), structure A is preferable for inductive components to achieve low loss. Narrower (higher impedance) lines are especially desirable.

The structure B reflection coefficient of the open stub, which represents the capacitor characteristics, extended farther out

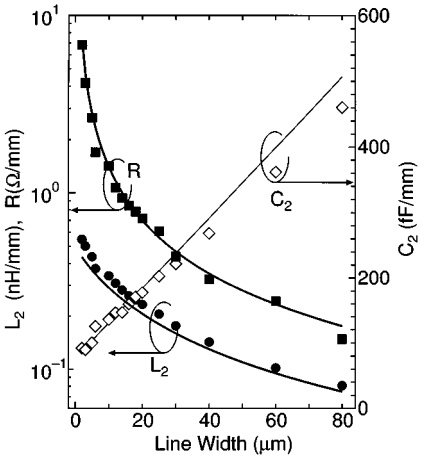


Fig. 5. Calculated and extracted equivalent circuit parameters for the structure B transmission lines. The solid lines show the calculated parameters, and the marks show the parameters extracted from the measured s-parameters.

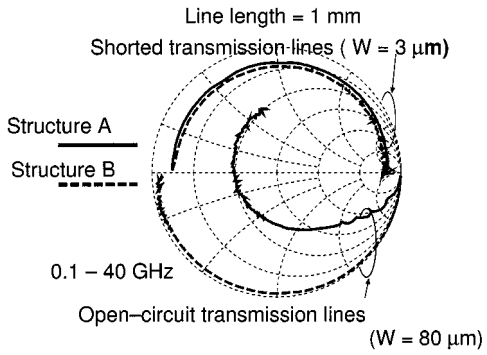


Fig. 6. Smith chart showing measured reflection coefficients for shorted transmission lines with 3-μm-wide structures A and B, plotted in the upper part, and for open-circuit transmission lines with 80-μm-wide structures A and B, plotted in the lower part.

than the structure A reflection coefficient in the upper part of the Smith chart. Even though 8-μm-thick polyimide–SiON–SiO_2 isolation layers were used, the wide low-impedance structure A lines produced an excessive insulation capacitance. Thus, we applied wider (lower impedance) lines using structure B for the capacitive components.

B. Noise Properties

To analyze the noise properties of the transmission lines on an Si substrate, we treated a transmission line of a certain length as a π-type equivalent circuit [see Fig. 7(a)]. We considered not only the thermal noise er of the transmission-line series resistance r, but also the thermal noises $e\mathrm{sub1}$ and $e\mathrm{sub2}$ of the substrate spread resistances r_{sub}. Comparing the equivalent circuits of Fig. 7(a) and (b), we found the following equivalent input noise–voltage and noise–current generators of e and i [13]:

$$e = er - \frac{\omega c_i (r + j\omega l)}{\gamma} e\mathrm{sub2} \tag{3}$$

$$i = -\left(\frac{j\omega^2 c_i^2 r_{\mathrm{sub}}}{\gamma} - j\omega c_i - \frac{1}{r + j\omega l}\right) e - \frac{\omega c_i}{\gamma} e\mathrm{sub1} - \frac{1}{r + j\omega l} er \tag{4}$$

where γ is $(\omega r_{\mathrm{sub}}(c_i + c_{\mathrm{sub}}) - j)$.

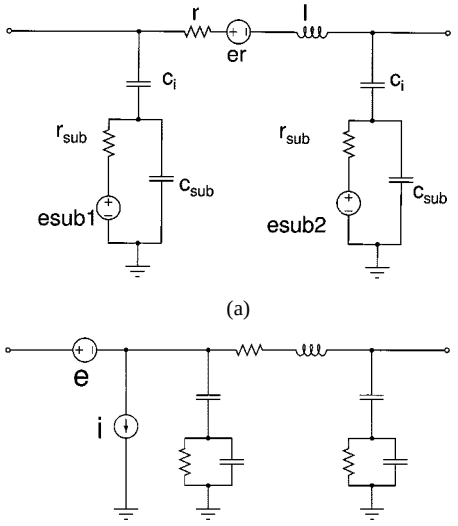


Fig. 7. (a) Equivalent circuit for a structure A transmission line of a certain length including thermal noise generated by the series resistance and substrate spread resistances. (b) To derive the NF of the transmission lines, the noise equivalent circuit in (a) was changed to an equivalent circuit composed of input equivalent noise generators and noiseless linear circuit elements.

The noise figure (NF) defined for a 50-Ω input-impedance signal source was calculated as

$$\mathrm{NF(dB)} = 10\log\left(\frac{\overline{i_s^2} + \overline{|i + e/50|^2}}{\overline{i_s^2}}\right) \tag{5}$$

where i_s is the signal-source noise current generated by a 50-Ω input impedance.

We measured the NF of a 10-μm-wide and 1-mm-long structure A transmission line (Fig. 8). The NF degraded rapidly as the frequency increased. The solid line is the calculated NF. The parameters were extracted data from the s-parameter measurement [see Fig. 4(a) and (b)] were used for the calculation. The frequency dependence of the measured NF agreed well with the calculated results. The NF degradation in the high-frequency range was due to noise from the substrate spread resistance r_{sub} coupling through the isolation capacitance c_i.

Fig. 9 shows the calculated NF relative to inductance for three types of transmission line at 15 GHz. The 3-μm-wide structure A line was better than the 10-μm-wide structure A line in terms of the NF because it was narrower and shorter and, thus, had lower isolation capacitance, even though it had higher resistance per unit length resistance. The NF for the 3-μm-wide structure B transmission line was higher than the NFs for the structure A transmission lines below 0.6 nH because the structure B transmission line was longer and had a higher resistance.

V. Amplifier Design and Performance

We demonstrated single-gate and cascode-connected Ku-band Si MOSFET amplifiers, both with on-chip matching networks. The circuit configurations are shown in Fig. 10. Since the conventional CMOS LSI process used does not include the metal–insulator–metal (MIM) capacitance process, we could not use capacitances in the signal paths for impedance matching. Therefore, we used open-stub configuration (low-pass type)

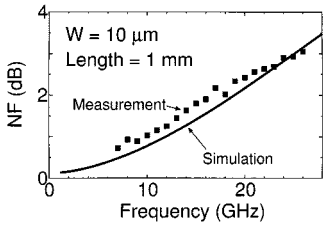


Fig. 8. Measured and simulated NF of a 10-μm-wide and 1-mm-long structure A transmission line.

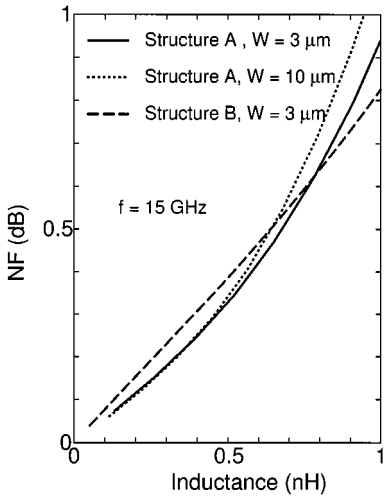


Fig. 9. Calculated NF versus inductance for 3-μm-wide structure A, 10-μm-wide structure A, and 3-μm-wide structure B transmission lines at 15 GHz.

matching networks. The matching networks were tuned to 50-Ω input and output impedances.

The gatewidths of the MOSFETs were 200 μm. We used 3-μm-wide high-impedance structure A inductive lines, where 3 μm is the minimum width of our thick Al metal patterning process, and 80-μm-wide low-impedance structure B capacitive lines, based on the transmission-line properties discussed above.

The high-impedance lines used for the input and output matching were 215–435-μm long, and their inductance was less than 0.6 nH. In particular, the inductance of the line used for input matching was less than 0.5 nH, thus, structure A was the better choice for a low-noise design. The low-impedance open stub lines used for the input and output matching were 456–500-μm long.

A chip photograph of the fabricated single-gate MOSFET MMIC is shown in Fig. 11. The interconnection lines between the probe pads and matching networks were structure B lines with a 50-Ω characteristic impedance.

A. s-Parameter Measurement

Fig. 12(a) shows the s-parameters of the single-gate MOSFET amplifier. It had a gain of 7.5–5 dB in the frequency range from 12 to 20 GHz at $V_{DD} = 2$ V and $V_G = 1$ V, with a 25-mA drain bias current when current saturation was achieved. As the return losses were below -10 dB from 17 to 21 GHz and S_{21} at 18 GHz was close to the MAG of the

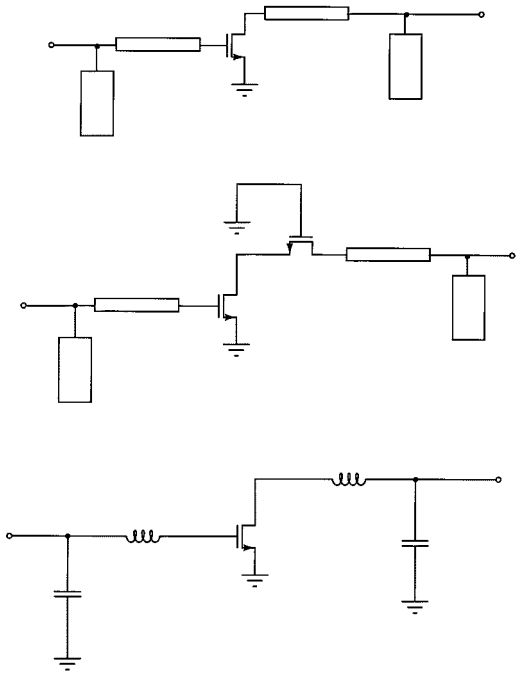


Fig. 10. (top) Single-gate MOSFET amplifier circuit. (middle) Cascode-connected MOSFET amplifier circuit. (bottom) Equivalent circuit for the single-gate MOSFET amplifier. The narrow lines use structure A, and act as inductors. The wide lines use structure B, and act as capacitors.

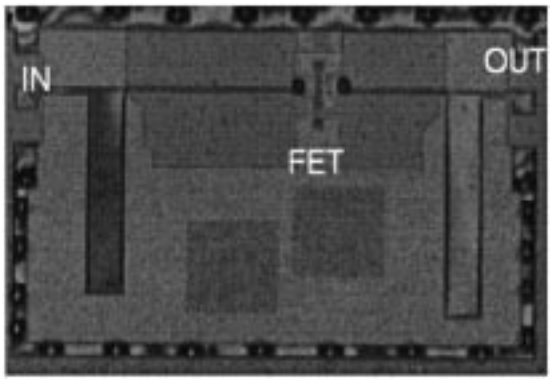


Fig. 11. Front view of the fabricated on-chip matched single-gate Si MOSFET amplifier.

circuit, the on-chip matching networks can provide excellent amplifier performance.

Fig. 12(b) shows the s-parameters of the cascode-connected MOSFET amplifier.V_{G1} refers to the gate voltage for the common-source stage and V_{G2} refers to that for the common-gate stage in the cascode configuration. The supplied drain voltage was 3 V, and the drain-bias current at $V_{G2} = 1.9$ V was 15.5 mA. The amplifier's gain was over 10 dB at about 23 GHz. However, the return losses were larger than expected. This is because neither a cascode-connected MOSFET equivalent circuit model, nor a large-signal MOSFET model were available when the amplifier was designed. A higher gain would be possible if the matching networks were more precisely tuned using a better MOSFET model.

The equivalent circuits of the MOSFET [see Fig. 1(a)] and the transmission lines [see Fig. 3(c) and (d)] on the Si substrate

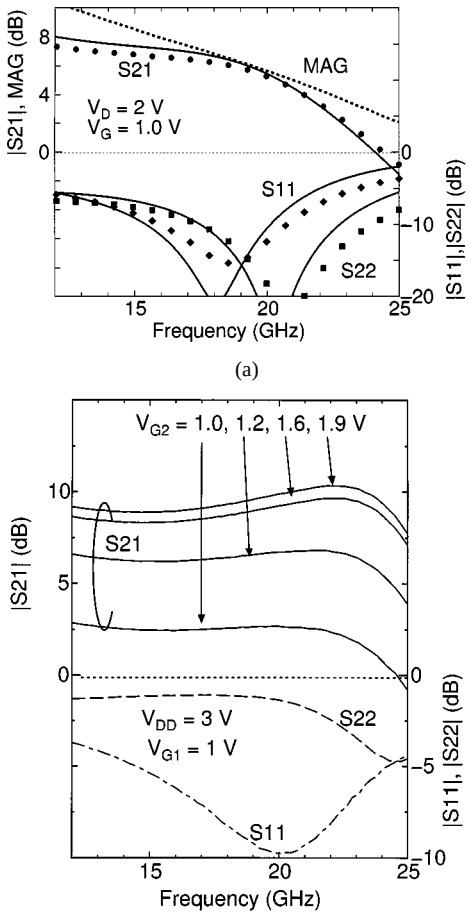


Fig. 12. (a) Measured and simulated performance of a fabricated on-chip matched amplifier with a single-gate MOSFET. The marks show the measured s-parameters, and the solid lines show the simulated results obtained using the small-signal equivalent circuits of the MOSFET and transmission lines. The MAG dashed line was calculated from the s-parameters of the measured amplifier. (b) Measured performance of a fabricated on-chip matched amplifier with cascoded MOSFETs. Return losses of $|S11|$ and $|S22|$ were obtained for $V_{G2} = 1.9$ V.

were modeled on the HP MDS high-frequency circuit simulator, and the results were used to calculate the s-parameters for the measured single-gate MOSFET amplifier. The solid lines inFig. 12(a) show simulated data. The predicted matching frequencies agreed with the measured values. Slight differences in $|S21|$ may have arisen from differences in the MOSFET gain between the model and the actual characteristics shown in Fig. 1(a). To verify our amplifier's performance improvement, we simulated the gain of an amplifier with second-level metal on-chip inductors (conventionally processed amplifier). The measured gain was 1.5 dB larger than the simulated gain of the conventionally processed amplifier.

B. NF Measurement

Fig. 13(a) shows the measured NF at 50 Ω for the single-gate MOSFET amplifier. It was 3.5–3.8 dB in the frequency range from 12 to 19 GHz. We believe this NF is the lowest yet reported for an Si MOSFET amplifier in the frequency range above 10 GHz [6].

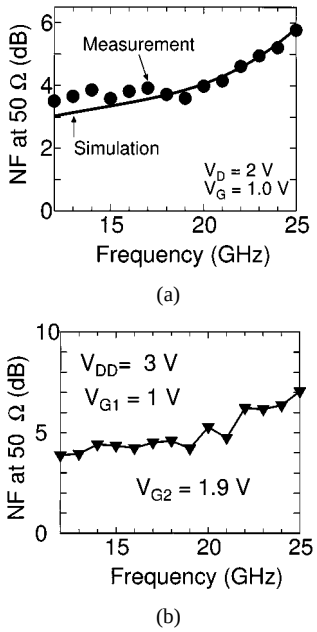


Fig. 13. (a) Measured simulated NFs at 50 Ω for the single-gate MOSFET amplifier. (b) Measured NFs at 50 Ω for the cascoded MOSFET amplifier.

The NF of the cascode-connected MOSFET amplifier is shown in Fig. 13(b). The NF in the frequency range between 12–20 GHz was 4 dB at a V_{G2} of 1.9 V. The NF of the cascode-connected MOSFET amplifier was worse than that of the single-gate MOSFET amplifier, possibly because—judging from the smaller bias current compared to the single-gate MOSFET measurement—the common-source stage MOSFET may not have been biased in the drain current saturation region [18].

Using the extrapolated FET and transmission-line noise parameters, we simulated the NF for the single-gate MOSFET amplifier. The simulated result, shown by the solid line in Fig. 13(a), agreed with the measured data quite well.

Judging from the simulation, such low-noise characteristics result from the low capacitance c_1 due to the thick polyimide–SiON–SiO_2 layers and the use of a minimum linewidth.

VI. Conclusions

In this paper, we evaluated a 0.18-μm-gatelength MOSFET and demonstrated its suitability for Ku-band applications. The MOSFET was modeled in terms of amplifier design using the small-signal model, including the Pospieszalski noise model. Transmission lines were formed from a 3-μm-thick Al metal layer on 8-μm-thick polyimide–SiON–SiO_2 layers on a lossy Si substrate. The lines were characterized and modeled.

Based on the modeling, we designed on-chip matched MOSFET amplifiers and demonstrated that they offer excellent gain and noise performance in the Ku-band. Although two additional fabrication processes were required, these processes are established and compatible with standard CMOS very large scale integration (VLSI) processes. Therefore, lower chip costs can be achieved by using Si substrates. Merging high-density

digital LSI circuits with RF analog signal-processing ICs thus appears to be practical up to the Ku-band.

ACKNOWLEDGMENT

The authors wish to thank H. Nozue, ULS Device Development, NEC Electron Devices, NEC Corporation, Kanagawa, Japan, F. Tamura, ULS Device Development, NEC Electron Devices, NEC Corporation, Kanagawa, Japan, H. Miyamoto, ULS Device Development, NEC Electron Devices, NEC Corporation, Kanagawa, Japan, K. Yoshida, ULS Device Development, NEC Electron Devices, NEC Corporation, Kanagawa, Japan, N. Tanabe, Silicon Systems Research Laboratories, NEC Corporation, Kanagawa, Japan, T. Hirota, Silicon Systems Research Laboratories, NEC Corporation, Kanagawa, Japan, T. Takeuchi, Silicon Systems Research Laboratories, NEC Corporation, Kanagawa, Japan, S. Kobayashi, Silicon Systems Research Laboratories, NEC Corporation, Kanagawa, Japan, and S. Saitoh, Silicon Systems Research Laboratories, NEC Corporation, Kanagawa, Japan, for their support in the device fabrication processes. The authors are also grateful to Dr. M. Ogawa, System Devices and Fundamental Research, NEC Corporation, Kanagawa, Japan, Dr. H. Abe, System Devices and Fundamental Research, NEC Corporation, Kanagawa, Japan, Dr. K. Honjo, System Devices and Fundamental Research, NEC Corporation, Kanagawa, Japan, Dr. H. Hida, System Devices and Fundamental Research, NEC Corporation, Kanagawa, Japan, and Dr. T. Kunio, System Devices and Fundamental Research, NEC Corporation, Kanagawa, Japan, for their advice and encouragement throughout this paper's research.

REFERENCES

[1] T. Yamamoto *et al.*, "High-frequency characteristics and its dependence on parasitic components in 0.1 μm Si–MOSFETs," in *IEEE VLSI Tech. Symp. Dig.*, 1996, p. 136.

[2] A. Tanabe, M. Soda, Y. Nakahara, T. Tamura, K. Yoshida, and A. Furukawa, "A single chip 2.4Gb/s CMOS optical receiver IC with low substrate crosstalk pre-amplifier," *IEEE J. Solid-State Circuits*, vol. 33, pp. 2148–2153, Dec. 1998.

[3] I. Toyoda, K. Nishikawa, T. Tokumitsu, K. Kamogawa, C. Yamaguchi, M. Hirano, and M. Akikawa, "Three-dimensional masterslice MMIC on Si substrate," *IEEE Trans. Microwave Theory Tech.*, vol. 45, pp. 2543–2530, Dec. 1997.

[4] N. Suematsu, M. Ono, S. Kubo, Y. Iyama, and O. Ishida, "L-band internally matched Si MMIC front-end," *IEEE Trans. Microwave Theory Tech.*, vol. 44, pp. 2375–2378, Dec. 1996.

[5] C. Rheinfelder, K. Strohm, F. Beisswanger, J. Gerdes, F. J. Schmuckle, J.-F. Luy, and W. Heinrich, "26 GHz coplanar SiGe MMIC's," in *IEEE Microwave Millimeter-Wave Monolithic Circuits Symp. Dig.*, San Francisco, CA, June 1996, pp. 205–208.

[6] Y.-C. Ho, K.-H. Kim, B. A. Floyd, C. W. Yuan Taur, I. Lagado, and K. K. O, "4- and 13-GHz tuned amplifiers implemented in a 0.1 μm CMOS technology on SOI, SOS, and bulk substrates," *IEEE J. Solid-State Circuits*, vol. 33, pp. 2066–2073, Dec. 1998.

[7] A. Higashisaka and T. Mizuta, "20-GHz band monolithic GaAs FET low-noise amplifier," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-29, pp. 1–6, Jan. 1981.

[8] Y. Nakahara, H. Yano, T. Hirayama, N. Matsuno, Y. Suzuki, and A. Furukawa, "Impact of interconnect capacitance reduction on RF–Si device performance," in *IEDM Tech. Dig.*, 1999, pp. 861–864.

[9] H. Yano, Y. Nakahara, T. Hirayama, N. Matsuno, Y. Suzuki, and A. Furukawa, "Ku-band Si MOSFET monolithic amplifiers with low-loss on-chip matching networks," in *RF IC Symp. Dig.*, 1999, pp. 127–130.

[10] M. W. Pospieszalski, "Modeling of noise parameters of MESFET's and MODFET's and their frequency and temperature dependence," *IEEE Trans. Microwave Theory Tech.*, vol. 37, pp. 1340–1350, Sept. 1989.

[11] G. Dambrine, J.-P. Raskin, F. Danneville, D. Vanhoenacker-Janvier, J.-P. Colinge, and A. Cappy, "High-frequency four noise parameters of silicon-on-insulator-based technology MOSFET for the design of low-noise RF integrated circuits," *IEEE Trans. Microwave Theory Tech.*, vol. 46, pp. 1733–1741, Aug. 1999.

[12] H. Hasegawa, M. Furukawa, and H. Yanai, "Properties of microstrip line on Si–SiO_2 system," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-19, pp. 869–881, Nov. 1971.

[13] R. Ludwig and P. Bretchko, *RF Circuit Design, Theory and Applications*. Englewood Cliffs, NJ: Prentice-Hall, 2000, p. 620.

[14] M. V. Schneider, "Microstrip lines for microwave integrated circuits," *Bell Syst. Tech. J.*, vol. 48, pp. 1421–1444, May-June 1969.

[15] H.-T. Yuan, Y.-T. Lin, and S.-Y. Chiang, *IEEE Trans. Electron Devices*, vol. ED-29, pp. 639–644, Apr. 1982.

[16] H. Hara, "Elementary circuit technology of MOS ULSI's" (in Japanese), in *Kindaikagakusya*, 1992, p. 224.

[17] T. Shibata and E. Sano, "Characterization of MIS structure coplanar transmission lines for investigation of signal propagation in integrated circuits," *IEEE Trans. Microwave Theory Tech.*, vol. 38, pp. 881–890, July 1990.

[18] C. A. Liechti, "Performance of dual-gate GaAs MESFET's as gain-controlled low-noise amplifiers and high-speed modulators," *IEEE Trans. Microwave Theory Tech.*, vol. MTT–23, pp. 461–469, June 1975.

Hitoshi Yano was born in Hokkaido, Japan, in 1962. He received the B.E. and M.E. degrees in electrical engineering from Hokkaido University, Hokkaido, Japan, in 1985 and 1987, respectively.

In 1987, he joined Microelectronics Research Laboratories, NEC Corporation, Kawasaki, Japan. From 1987 to 1994, he was engaged in the research and development of GaAs FET devices, especially in development of two-dimensional device simulation technology. Since 1994, he has been involved with designs of GaAs heterojunction and CMOS MMICs in the Photonic and Wireless Devices Research Laboratories, System Devices and Fundamental Research, NEC Corporation, Ibaraki, Japan.

Mr. Yano is a member of the Institute of Electronics, Information and Communication Engineers (IEICE), Japan and the Japan Society of Applied Physics.

Yasushi Nakahara received the B.E. and M.E. degrees in electrical engineering from Keio University, Tokyo, Japan, in 1992 and 1994, respectively.

In 1994, he joined the Microelectronics Research Laboratories, NEC Corporation, Kawasaki, Japan, where he is currently engaged in the research and development of scaled silicon MOSFETs and high-speed communication ICs.

Mr. Nakahara is a member of the Japan Society of Applied Physics.

Tomohisa Hirayama received the B.S. and M.S. degrees in applied physics from the University of Tokyo, Tokyo, Japan, in 1994 and 1996, respectively.

Since 1996, he has been with the Microelectronics Research Laboratories, NEC Corporation, Kawasaki, Japan, where he has been engaged in research and development of MOSFETs and heterojunction bipolar transistors (HBTs) for power devices. He is currently a member of the Photonic and Wireless Devices Research Laboratories, System Devices and Fundamental Research, NEC Corporation, Ibaraki, Japan.

Mr. Hirayama is a member of Institute of Electronics, Information and Communication Engineers (IEICE), Japan.

Noriaki Matsuno was born in 1968. He received the B.E. and M.E. degrees in electrical engineering from Nagoya University, Nagoya, Japan, in 1991 and 1993.

In 1993, he joined the Microelectronics Research Laboratories, NEC Corporation, Kawasaki, Japan, where he was engaged in research and development for high-speed and low-power consumption LSIs with GaAs-based heterostructure FETs. He was involved in the research and development for Si-based microwave devices and circuits. Since 2000, he has been with the Photonic and Wireless Devices Research Laboratories., System Devices and Fundamental Research, NEC Corporation.

Mr. Matsuno is a member of the Japan Society of Applied Physics.

Yasuyuki Suzuki was born in Toyama, Japan, on December 24, 1959. He received the B.E. and M.S. degrees in engineering science and scientific technology from the University of Tsukuba, Ibaraki, Japan, in 1982 and 1984, respectively.

In 1984, he joined the Microelectronics Research Laboratories, NEC Corporation, Kawasaki, Japan, where he was engaged in research and development of low-noise heterojunction FETs and high-speed heterojunction FET ICs. From 1992 to 1994, he was engaged in the development of optical-fiber communication systems. He is currently a Manager of the Photonic and Wireless Devices Research Laboratory, System Devices and Fundamental Research, NEC Corporation, Ibaraki, Japan, where he has been engaged in research and development of high-speed ICs and MMICs for optical communications and wireless communications.

Dr. Suzuki is a member of the Institute of Electronics, Information and Communication Engineers (IEICE), Japan.

Akio Furukawa received the B.S., M.S., and Ph.D. degrees in physics from the University of Tokyo, Tokyo, Japan, in 1979, 1981, and 1984, respectively.

In 1985, he joined the NEC Corporation, where he was engaged in research on molecular-beam-epitaxial growth, and HBTs and FETs of compound semiconductors, scaled CMOS, and technology computer-aided design (TCAD). He is currently the Manager of the Photonic and Wireless Devices Research Laboratories, System Devices and Fundamental Research, NEC Corporation, Ibaraki, Japan.

Dr. Furukawa is a member of the Japan Society of Applied Physics.